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Lfw



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Michael Rogers Lambert, et al.

Serial No.: 10/806485

Examiner: Unknown

Filing Date: Mar 22, 2004

Group Art Unit: 2133

Title: Scan Test Tools, Models And/ Or Methods

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- (a) ☐ Under 37 CFR 1.97(b).
(Within three months of filing national application; or date of entry of national application; or before mailing date of first Office action on the merits; whichever occurs last).
- (b) ☒ Under 37 CFR 1.97(c) together with *either* a:
☒ Statement under CFR 1.97(e), or
☐ \$180.00 fee under 37 CFR 1.17(p).
(After the CFR 1.97(b) time period, but before a final action or notice of allowance, whichever occurs first).
- (c) ☐ Under 37 CFR 1.97(d) together with: a
Statement under 37 CFR 1.97(e), *and*
\$180.00 fee as set forth in 37 CFR 1.17(p).
(After a final action or notice of allowance, whichever occurs first, but before payment of the issue fee).

☒ STATEMENT UNDER 37 CFR 1.97(e)

The undersigned certifies that:

- ☒ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the statement, or
- ☐ No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 CFR § 1.56(c) more than three months prior to the filing of the Information Disclosure Statement.

☐ PRIOR APPLICATIONS

References identified with an asterisk (*) in the enclosed PTO Form 1449, were disclosed in prior Patent Application No. _____, filed _____, now U.S. Patent No. _____, and, as such, copies thereof are not included pursuant to the provisions of 37 CFR 1.98(d).

☐ FOREIGN LANGUAGE DOCUMENTS

A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO form 1449, as presently understood by the individual(s) designated in 37 CFR 1.56(c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

☒ **FEE AUTHORIZATION**

Please charge to Deposit Account **50-1078** the sum of \$0.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-1078** pursuant to 37 CFR 1.25.

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☐ I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Date of Facsimile:

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Respectfully submitted,

Michael Rogers Lambert, et al.

By

Floyd E. Anderson
Floyd E. Anderson
Attorney/Agent for Applicant(s)

Reg. No. 33,825

Date: 2 Sept 2005

Telephone No. 970 679 3242



Form PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTORNEY DOCKET NO.
10030245-01SERIAL NO.
10/806485

APPLICANT

Michael Rogers Lambert, et al.

FILING DATE

March 22, 2004

GROUP

2133

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME

FOREIGN PATENT DOCUMENT

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES NO	
	GE	2318876A	05/06/1998	Subhrajit Bhattacharya, et al.	x	
	WI	03/067272 A1	01/16/2003	Laung-Terng Wang, et al.	x	
	WI	03/052641 A1	11/29/2002	Benoit Nadeau-Dostie	x	

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

		"A CMOS Mixed-Signal Integrated Circuit Having A Reduced Vector Set And Closed-Loop Analog Test Architecture". By: A.V. Chavan, D.W. Stringfellow, S.R. Mallarapu, and R. Ardeishar. pp 471-474. IEEE 1996 Custom Integrated Circuits Conference.

EXAMINER

DATE CONSIDERED

* Copies of these references are not enclosed Pursuant to 37 CFR 1.98(d). (See accompanying IDS)

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